IN THE CLAIMS

1. (Amended) A memory system that receives addresses corresponding to data in an order comprising:

an address buffer that receives addresses in said order;

a memory array;

a control circuit that selects at a given cycle a memory reference from a set of pending memory references in said address buffer to present to the memory array, said references being presented to said memory array as they leave the control circuit in an order different than the order in which they were received; and

a read buffer, that receives data read out from the memory array.

2. A memory system according to claim 1 wherein said control circuit causes the read buffer to read out data from the read buffer in said order with respect to read requests.

3. A memory system according to claim 1 wherein the control circuit performs multiple accesses in sequential cycles to a given row in the memory in the order in which the addresses corresponding to the given row were received.

4. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs multiple accesses in sequential cycles to an active row of a given bank before activating a different row of the given bank.

5. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs multiple accesses in sequential cycles to an active row of a given bank before activating a different bank.

6. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs a row access to a currently inactive bank when another bank contains a currently active row.

B1 7. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks and the address buffer is partitioned into a separate address buffer for each bank.

8. A memory system according to claim 1 wherein said control circuit comprises:

a comparator for each address capable of being stored in the address buffer which compares the row address of each address with the row address of the currently active row; and

a priority encoder that selects the first address entered into the address buffer that is contained in the currently active row.

9. A memory system according to claim 1 wherein, associated with the read buffer is a head pointer and a tail pointer to assist in tracking the order sequence of read access requests, and a buffer array containing a status flag for each read access request having an associated address currently stored in the address buffer.

10. A memory system according to claim 1 wherein, during each of a plurality of sequential cycles, the address buffer inputs a new address and the control circuit compares the new address to the address of the currently active row.

11. A memory system according to claim 7 wherein, during each of a plurality of sequential cycles, the address buffer inputs a new address and the control circuit compares the new address to the address of the currently active row if the currently active row is in the same bank as the new address.

12. A memory system according to claim 11 wherein, if the address buffer inputs the new address and the new address does not correspond to the same bank as the address of the currently active row, the control circuit does not perform a comparison of the new address to the address of the currently active row.

13. (Amended) A method of accessing memory comprising the steps of:

receiving a sequential plurality of memory access requests in the form of an address inputs;

buffering the plurality of address inputs;

B1 initiating an out of order memory access request to a memory array for one of the sequential plurality of memory access requests such that one of the plurality of address inputs is requested in an order different than the order in which the one address was received;

selecting at a given cycle a memory reference from among a set of pending memory references and presenting this memory reference to said memory array; and

buffering read results of those memory access requests corresponding to read operations.

14. A method according to claim 13 wherein said step of initiating initiates the out of order memory access request initiates said request to an address having a row corresponding to a currently active row.

15. A method according to claim 13 wherein the buffered read results are read out in the in the order that the original read requests were made.

16. A method according to claim 13 wherein multiple accesses in sequential cycles to a given row in the memory array are made in the order in which the addresses. corresponding to the given row were received.

17. A method according to claim 13 wherein a plurality of row accesses are performed out of order to a currently active row before another row is made currently active.

18. A method according to claim 13 wherein the memory array is partitioned into a plurality of banks, and a row access is performed on a row of a currently inactive bank when another bank contains a currently active row.

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19. A method according to claim 13 wherein the step of buffering read results includes setting a read tail pointer to identify a next sequential location of a buffer and setting a read head pointer to remove data from the buffer.

Respectfully submitted,

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